

What is claimed:

1. A video processing circuit, comprising:  
a processor operable to:
  - 5 receive an encoded image having first and second regions;  
decode the first region of the image;  
modify the decoded first region; and  
re-encode the modified first region.
- 10 2. The video processing circuit of claim 1 wherein the processor is operable to combine the encoded second region of the image and the re-encoded first region of the image to generate an encoded modified image.
- 15 3. The video processing circuit of claim 1 wherein the processor is operable to:
  - decode the first region into a transform domain; and  
modify the decoded first region in the transform domain.
- 20 4. The video processing circuit of claim 1 wherein the processor is operable to:
  - decode the first region into a pixel domain; and  
modify the decoded first region in the pixel domain.
- 25 5. The video processing circuit of claim 1 wherein:
  - the first region has dimensions and a location within the image; and  
the processor is operable to receive the dimensions and location of the first region.
- 30 6. A video processing circuit, comprising:  
a processor operable to:
  - receive an encoded base image having first and second regions and  
an encoded overlay image;  
decode the overlay image and the first region of the base image;

combine the decoded overlay image with the decoded first region of the base image to form a modified first region of the base image; and re-encode the modified first region of the base image.

5           7.       The video processing circuit of claim 6 wherein the processor is operable to combine the encoded second region of the base image and the re-encoded modified first region of the base image to generate an encoded modified base image.

10           8.       The video processing circuit of claim 6 wherein the processor is operable to:  
              decode the overlay image and the first region of the base image into a transform domain; and  
              combine the decoded overlay image with the decoded first region of the base  
15       image in the transform domain.

              9.       The video processing circuit of claim 6 wherein the processor is operable to:  
              decode the overlay image and the first region of the base image into a pixel  
20       domain; and  
              combine the decoded overlay image with the decoded first region of the base image in the pixel domain.

              10.      The video processing circuit of claim 6 wherein the overlay image  
25       comprises a program guide.

              11.      The video processing circuit of claim 6, further comprising:  
              a buffer; and  
              wherein the processor is operable to store the encoded second region of the  
30       base image and the re-encoded modified first region of the base image in a buffer as an encoded modified base image.

12 A video processing circuit, comprising:

a display output;

a processor operable to receive an encoded base image having first and second regions, an encoded overlay image, and an overlay signal, the processor coupled to the display output and operable to perform the following steps in response to the overlay signal:

decode the overlay image and the first region of the base image;

combine the decoded overlay image with the decoded first region of the base image to form a modified first region of the base image;

re-encode the modified first region of the base image;

combine the encoded second region of the base image and the re-encoded modified first region of the base image to form an encoded modified base image; and

provide the encoded modified base image on the display output; and

the processor operable to provide the encoded base image on the display output in the absence of the overlay signal.

13. The video processing circuit of claim 12 wherein the overlay image comprises a program guide.

14. The video processing circuit of claim 12 wherein the overlay signal comprises a remote-control overlay signal.

15. The video processing circuit of claim 12, further comprising:

a buffer; and

wherein the processor is operable to combine the encoded second region of the base image and the re-encoded modified first region of the base image by storing the encoded second region and the re-encoded modified first region in the buffer.

**16/ A video processing circuit, comprising:**

4 a processor operable to receive encoded images each having respective first and second regions, each of the first and second regions divided into respective image subregions, the processor programmed to:

5        decode at least one of the image subregions in the first region of an image;  
       modify the decoded image subregion; and  
       re-encode the modified image subregion.

17. The video processing circuit of claim 16 wherein the processor is  
10 programmed to re-encode the modified image subregion as an intra-coded  
subregion.

18. The video processing circuit of claim 16 wherein the processor is  
programmed to re-encode the modified image subregion as non-intra-coded  
15 subregion having a motion vector with a location value of zero.

19. The video processing circuit of claim 16 wherein the processor is operable to:

20       receive an overlay image divided into overlay subregions;  
      decode at least one of the overlay subregions;  
      modify the decoded image subregion by combining the decoded image  
      subregion with the decoded overlay subregion to form the modified image subregion;  
      and

re-encode the modified image subregion by intra-coding the modified image  
25 subregion.

20. The video processing circuit of claim 16 wherein the processor is operable to:

30       receive an overlay image divided into overlay subregions;  
      decode at least one of the overlay subregions;  
      modify the decoded image subregion by combining the decoded image  
      subregion with the decoded overlay subregion to form the modified image subregion;  
      and

re-encode the modified image subregion as a non-intra-coded subregion having a motion vector with a location value of zero.

21. The video processing circuit of claim 16 wherein the processor is  
5 operable to:

receive overlay images divided into respective overlay subregions, the overlay images having a scroll rate;

decode at least one of the overlay subregions;

10 modify the decoded image subregion by combining the decoded image subregion with the decoded overlay subregion to form the modified image subregions; and

re-encode the modified image subregion as non-intra-coded subregion having a motion vector with a value based on the scroll rate.

15 22. The video processing circuit of claim 16 wherein the image subregions each comprise a respective macro block.

~~23.~~ A video processing circuit, comprising:

~~a display output;~~

20 a processor coupled to the display output and operable to:

receive a sequence of encoded images each having respective first and second regions, the sequence including intra-coded and non-intra-coded images;

decode the first region of an intra-coded image;

25 modify the decoded first region;

re-encode the modified first region;

combine the encoded second region of the intra-coded image and the re-encoded modified first region of the intra-coded image to form an encoded modified intra-coded image; and

30 provide the encoded modified intra-coded image on the display output.

24. The video processing circuit of claim 23 wherein the processor is operable to uncouple the respective first and second regions of the non-intra-coded images from the display output.

5 25. The video processing circuit of claim 23 wherein the processor is operable to uncouple the respective second regions of the non-intra-coded images from the display output.

10 26. The video processing circuit of claim 23 wherein the processor is operable to:  
decode the first region of a non-intra-coded image;  
modify the decoded first region of the non-intra-coded image;  
re-encode the modified first region of the non-intra-coded image;  
15 combine the encoded second region of the intra-coded image and the re-encoded modified first region of the non-intra-coded image to form an encoded modified image; and  
provide the encoded modified image on the display output.

20 27. A video processing circuit, comprising:  
a processor operable to:  
receive an encoded image having first and second regions;  
decode the first and second regions;  
change the resolution of the first and second regions;  
25 modify the first region after changing its resolution; and  
re-encode the modified first region.

28. The video processing circuit of claim 27 wherein the processor is operable to change the resolution by reducing the resolution of the first and second regions.

30 29. The video processing circuit of claim 27 wherein the processor is operable to combine the encoded second region of the image and the re-encoded first region of the image to generate an encoded modified image.

30. The video processing circuit of claim 27 wherein the processor is operable to change the resolution of the first and second regions in the transform domain.

5

31. A video processing circuit, comprising:  
a processor operable to:

receive an encoded base image and an encoded overlay image;

decode the base image and the overlay image; and

10 combine the decoded base image and the decoded overlay image in the transform domain to form a modified image.

32. The video processing circuit of claim 31 wherein the processor is further operable to re-encode the modified image.

15

33. The video processing circuit of claim 31 wherein the processor is operable to combine the decoded base and overlay images by alpha blending the decoded base image and the decoded overlay image.

20 34. The video processing circuit of claim 6 wherein the overlay image comprises a program guide.

35. The video processing circuit of claim 6 wherein the base image comprises a video frame.

25

36. A video processing circuit, comprising:  
a display output;

a processor coupled to the display output and operable to:

receive a sequence of intra-coded and non-intra-coded images; and

30 provide an intra-coded image from the sequence to the display output in place of at least one of the non-intra-coded images from the sequence.

37. The video processing circuit of claim 36 wherein the processor is further operable to:  
decode the intra-coded image;  
modify the decoded intra-coded image;  
5 re-encode the modified intra-coded image; and  
provided the re-encoded intra-coded image to the display output in place of at least one of the non-intra-coded images from the sequence.

10 ~~38.~~ A method, comprising:  
decoding a first region of an encoded image having the first region and a second region;  
modifying the decoded first region; and  
re-encoding the modified first region.

15 39. The method of claim 38, further comprising combining the encoded second region of the image and the re-encoded first region of the image to form an encoded modified image.

20 40. The method of claim 38 wherein:  
the decoding comprises decoding first region into a transform domain; and  
the modifying comprises modifying the decoded first region in the transform domain.

25 41. The method of claim 38 wherein:  
the decoding comprises decoding the first region into a pixel domain; and  
the modifying comprises modifying the decoded first region in the pixel domain.

30 ~~42.~~ A method, comprising:  
decoding an encoded overlay image and a first region of an encoded base image having the first region and a second region;



combining the decoded overlay image with the decoded first region of the base image to form a blended first region of the base image; and  
re-encoding the blended first region of the base image.

5           43.    The method of claim 42, further comprising:  
              combining the encoded second region of the base image and the re-encoded first region of the base image to form an encoded modified base image.

10           44.    The method of claim 42 wherein:  
              the decoding comprises decoding the overlay image and the first region of the base image into a transform domain; and  
              the combining comprises combining the decoded overlay image and the decoded first region in the transform domain.

15           45.    The method of claim 42 wherein:  
              the decoding comprises decoding the overlay image and the first region of the base image into a pixel domain; and  
              the combining comprises combining the decoded overlay image and the decoded first region in the transform domain.

20           ~~46.~~   A method, comprising:  
              an overlay mode, comprising:  
                  decoding an encoded overlay image and a first region of an encoded base image having the first region and a second region;  
25                combining the decoded overlay image with the decoded first region of the base image to form a modified first region of the base image;  
                  re-encoding the modified first region of the base image;  
                  combining the encoded second region of the base image and the re-encoded first region of the base image to form an encoded modified base  
30                image; and  
                  providing the encoded modified base image on a display output; and  
              a non-overlay mode, comprising providing the encoded base image on the display output.

47. The method of claim 46 wherein the overlay image comprises a program guide.

5

48. A method, comprising:

decoding at least one image subregion in a first region of an encoded image having the first region and a second region divided into respective image subregions; modifying the decoded image subregion; and re-encoding the modified image subregion.

10

49. The method of claim 48, further comprising:

receiving an overlay image divided into respective overlay subregions; decoding at least one of the overlay subregions; wherein the modifying comprises combining the decoded image subregion with the decoded overlay subregion to form the modified image subregion; and wherein the re-encoding comprises intra coding the modified image subregion.

15

50. The method of claim 48, further comprising:

receiving an overlay image divided into respective overlay subregions; decoding at least one of the overlay subregions; wherein the modifying comprises combining the decoded image subregion with the decoded overlay subregion to form the modified image subregion; and wherein the re-encoding comprises non-intra coding and generating a motion vector for the modified image subregion, the motion vector having a location value of zero.

20

51. The method of claim 48, further comprising:

receiving an overlay image divided into respective overlay subregions, the overlay images having a scroll rate; decoding at least one of the overlay subregions; wherein the modifying comprises combining the decoded image subregion with the decoded overlay subregion to form the modified image subregion; and

30

wherein the re-encoding comprises non-intra coding and generating a motion vector for the modified image subregion, the motion vector having a location value based on the scroll rate.

5        ~~52.~~ A method, comprising:

~~decoding a first region of an intra-coded image from a sequence of encoded intra-coded and non-intra-coded images each having respective first and second regions;~~

modifying the decoded first region;

10       re-encoding the modified first region;

combining the encoded second region of the intra-coded image and the re-encoded first region of the intra-coded image to form an encoded modified intra-coded image; and

providing the encoded modified intra-coded image to a display.

15

53. The method of claim 52, further comprising holding back the respective first and second regions of the non-intra-coded images from the display.

20       54. The method of claim 52, further comprising holding back the respective second regions of the non-intra-coded images from the display.

25       55. The method of claim 52, further comprising:

decoding the first region of a non-intra-coded image;

modifying the decoded first region of the non-intra-coded image;

25       re-encoding the modified first region of the non-intra-coded image;

combining the encoded second region of the intra-coded image and the re-encoded first region of the non-intra-coded image to form an encoded modified image; and

provide the encoded modified image to the display.

30

~~56.~~ A method, comprising:

~~receiving an encoded image having first and second regions;~~

~~decoding the first and second regions;~~

changing the resolution of the first and second regions;  
modifying the first region after changing its resolution; and  
re-encoding the modified first region.

5            57.    The method of claim 56 wherein the changing comprises reducing the  
resolution of the first and second regions.

10           58.    The method of claim 56, further comprising combining the encoded  
second region of the image and the re-encoded first region of the image to generate  
an encoded modified image.

15           59.    The method of claim 56 wherein the changing comprises changing the  
resolution of the first and second regions in the transform domain.

20           60.    A method, comprising:  
receiving an encoded base image and an encoded overlay image;  
decoding the base image and the overlay image; and  
combining the decoded base image and the decoded overlay image in the  
transform domain to form a modified image.

25           61.    The method of claim 60, further comprising re-encoding the modified  
image.

30           62.    The method of claim 60 wherein the combining comprises alpha  
blending the decoded base image and the decoded overlay image.

35           63.    A method, comprising:  
receiving a sequence of intra-coded and non-intra-coded images; and  
providing an intra-coded image from the sequence to a display device in place  
of at least one of the non-intra-coded images from the sequence.

